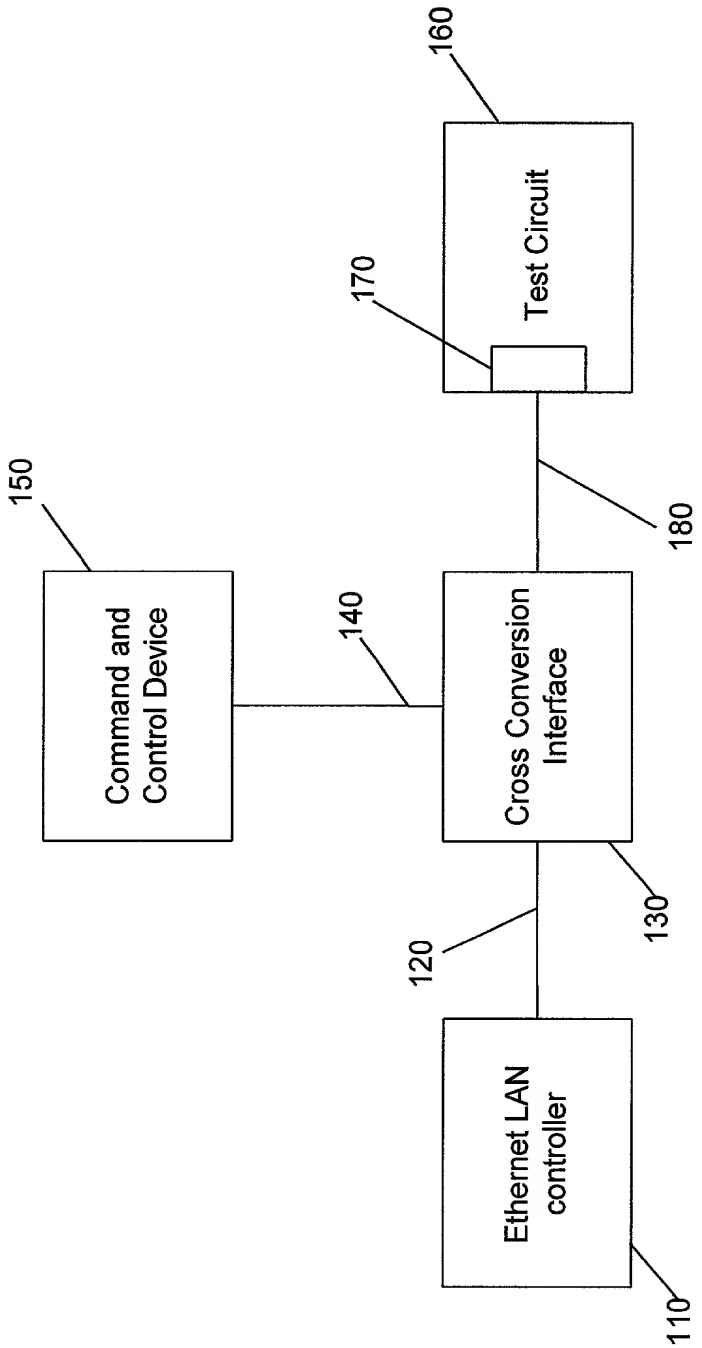
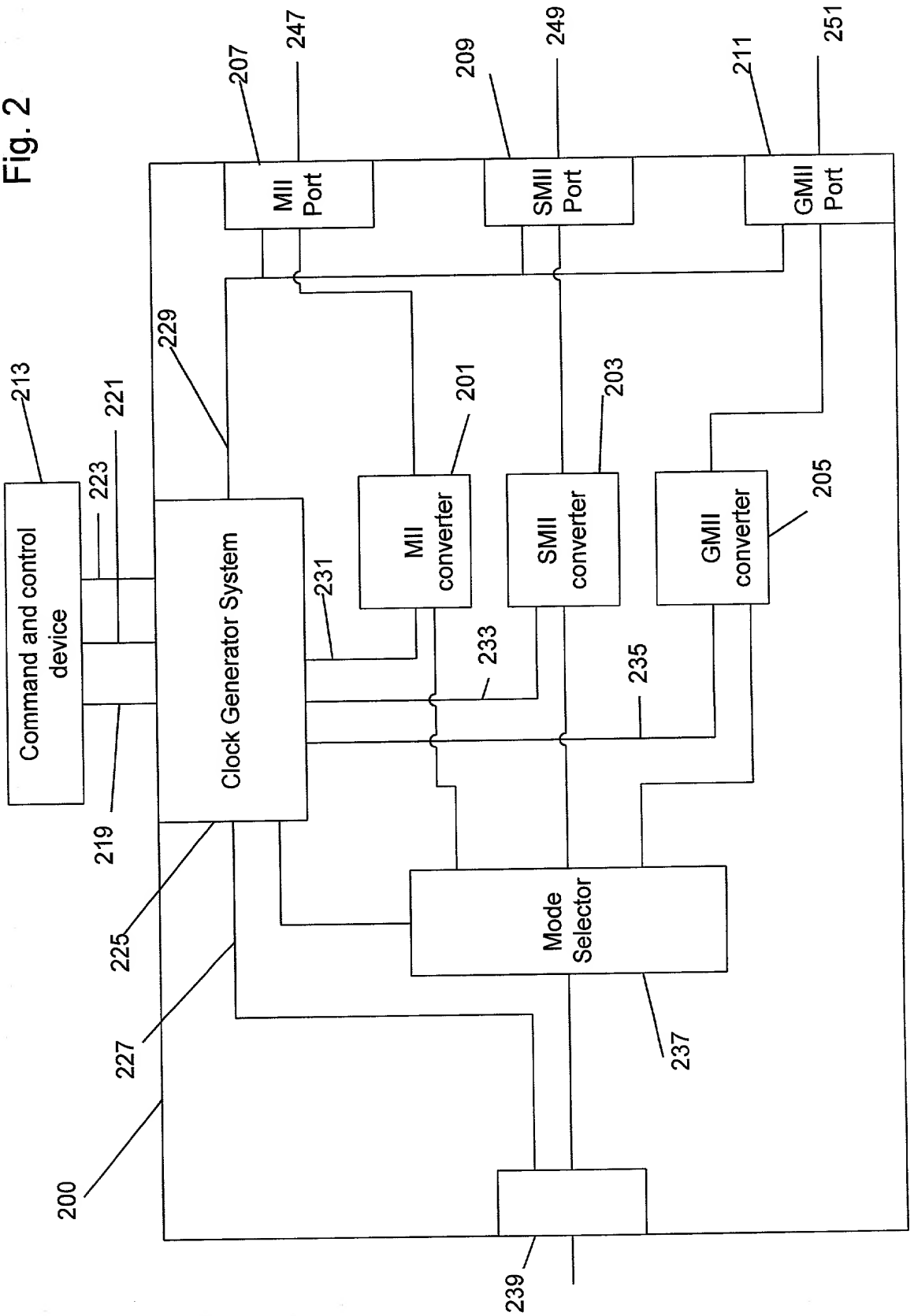

160
Test Circuit
170
150
180
Command and Control Device
140
Cross Conversion Interface
130
120
Ethernet LAN controller
110

Fig. 1

Fig. 2


MII Port
SMII Port
GMII Port
Command and control device
Clock Generator System
MII converter
SMII converter
GMII converter
Mode Selector
207
247
209
249
211
251
213
221
223
229
201
203
205
231
233
235
219
225
227
237
200
239

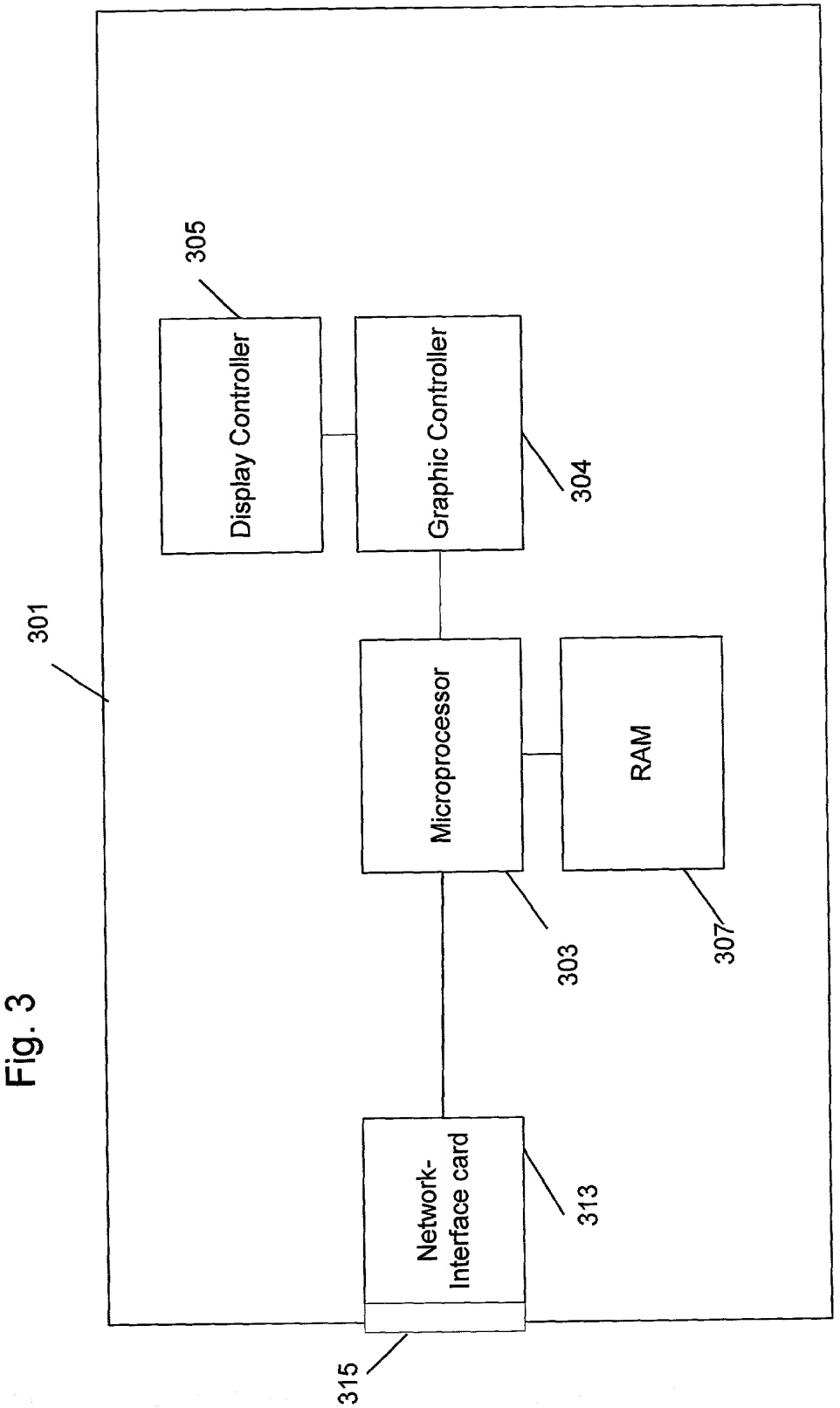

301
305
Display Controller
Graphic Controller
304
Microprocessor
RAM
303
307
Network-
Interface card
313
315
PRIOR ART

Fig. 3

Fig. 4

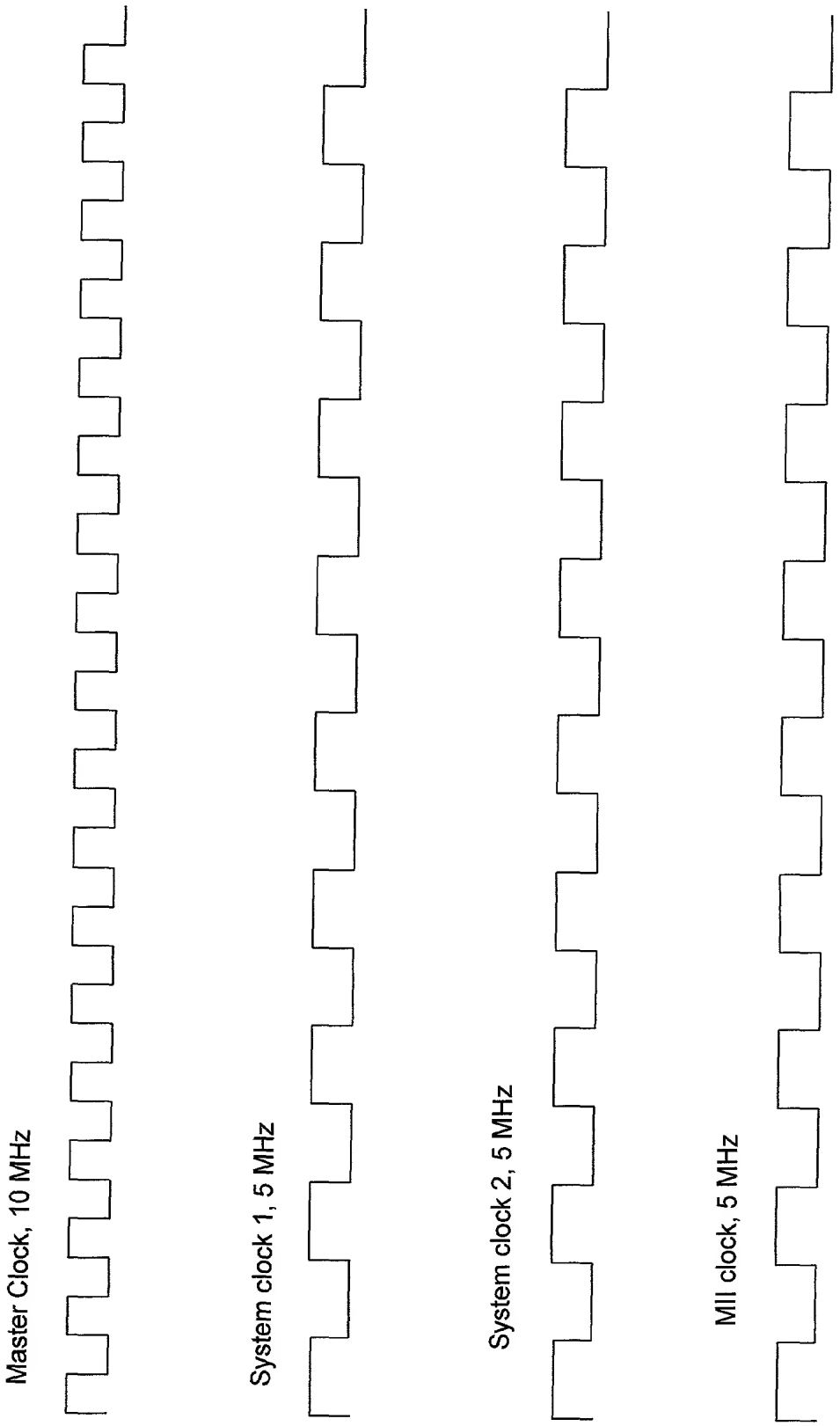

Master Clock, 10 MHz
System clock 1, 5 MHz
System clock 2, 5 MHz
MII clock, 5 MHz

Fig. 5

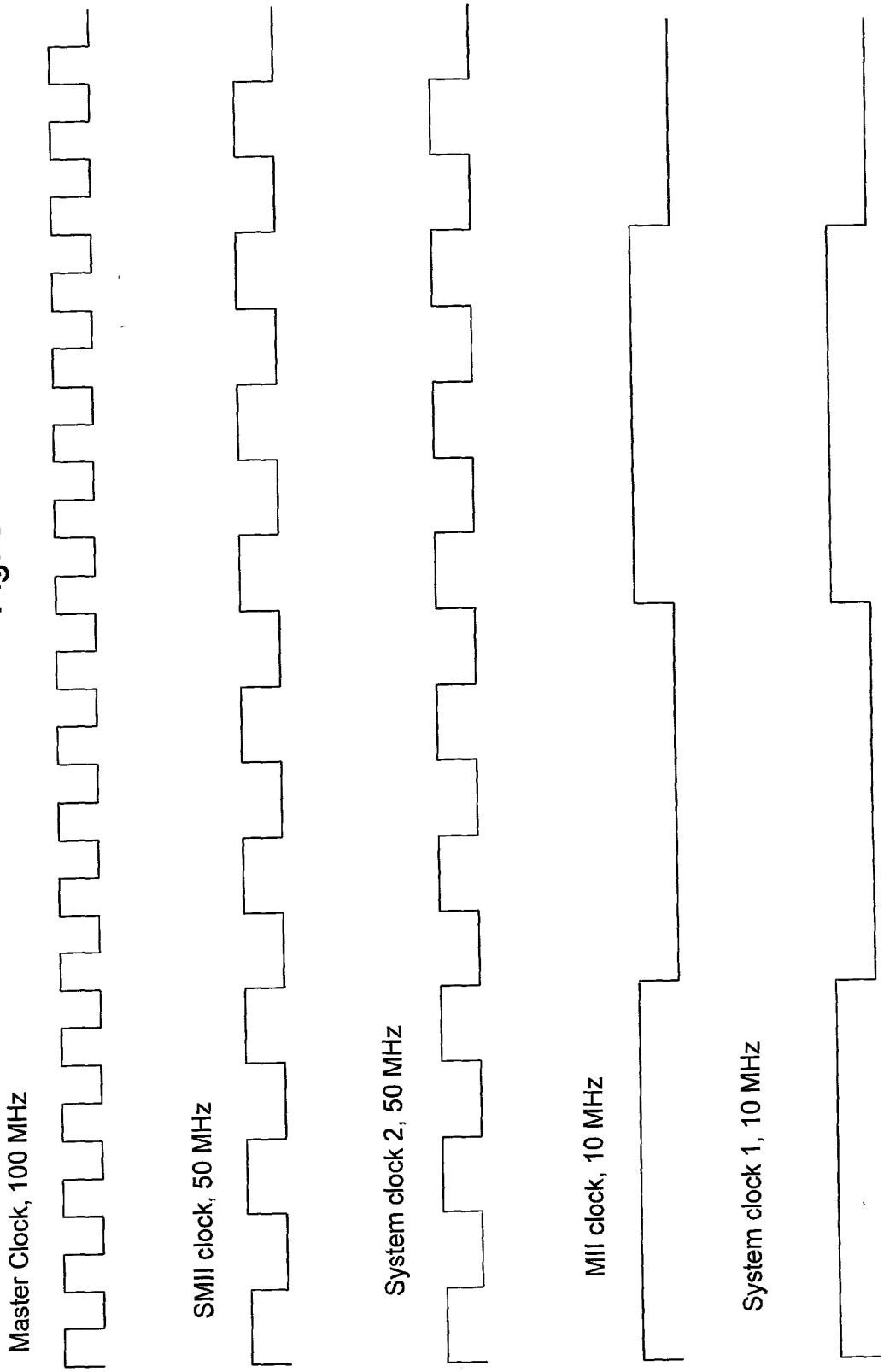

Master Clock, 100 MHz
SMII clock, 50 MHz
System clock 2, 50 MHz
MII clock, 10 MHz
System clock 1, 10 MHz

Fig. 6

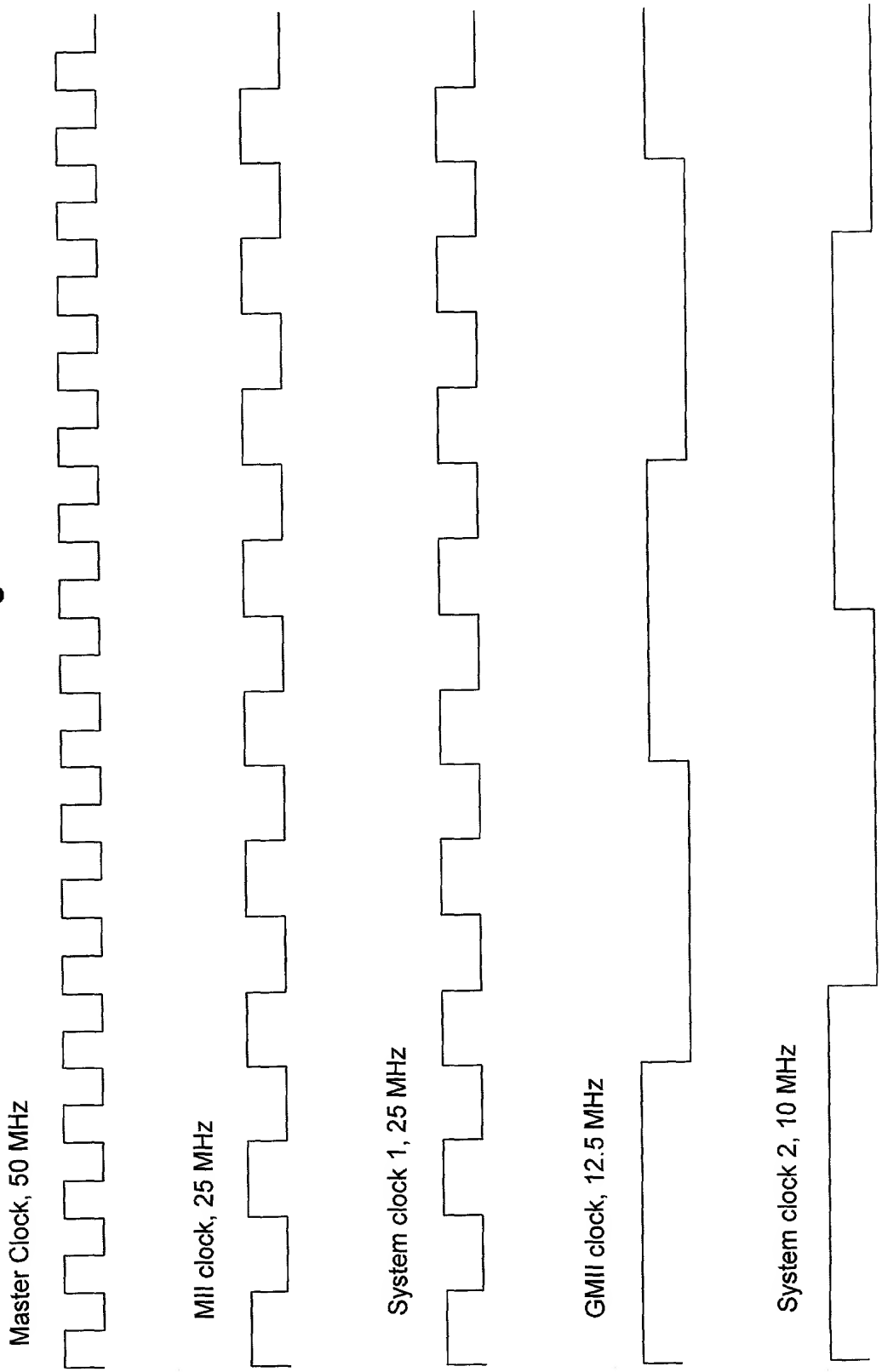
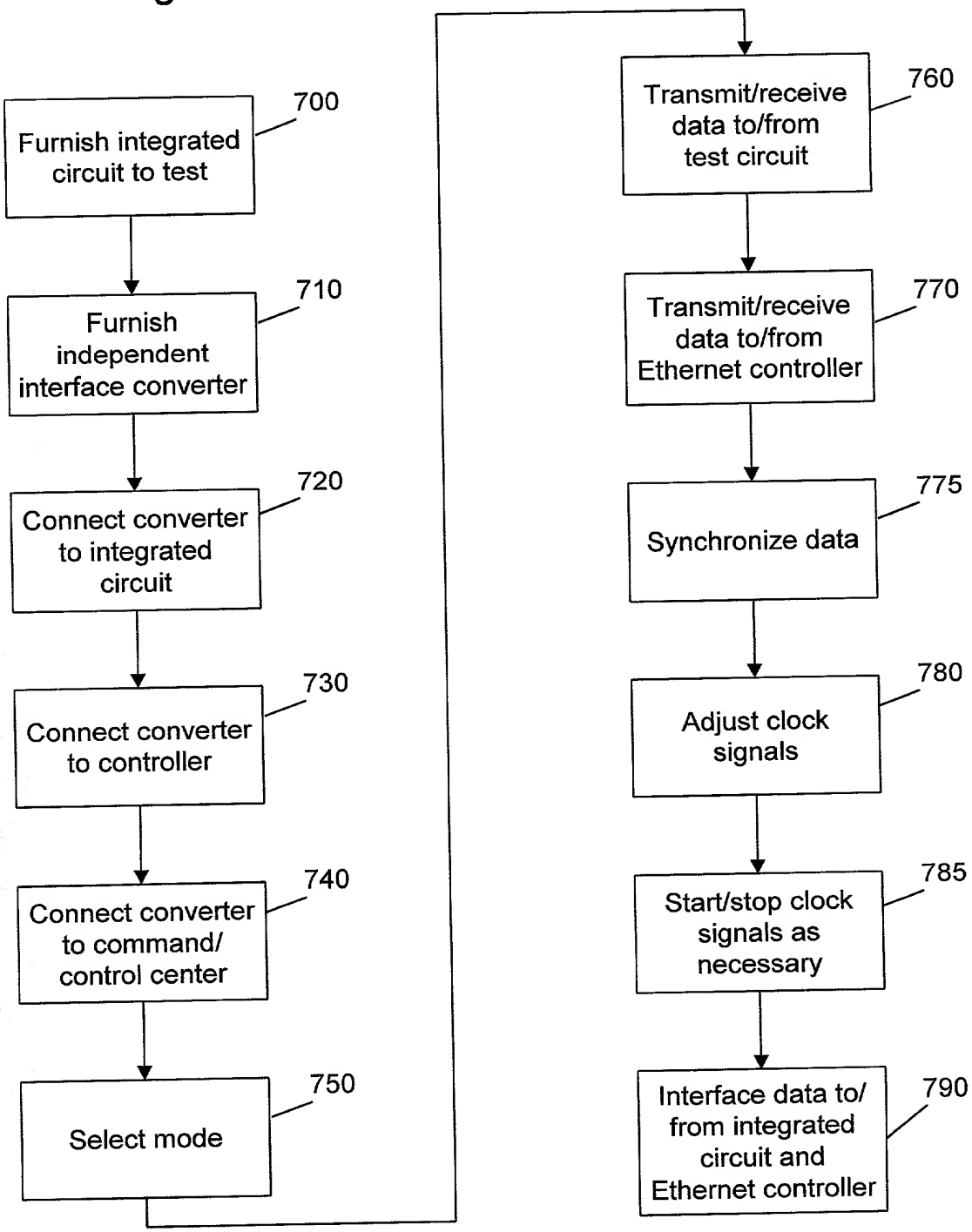

Master Clock, 50 MHz
MII clock, 25 MHz
System clock 1, 25 MHz
GMII clock, 12.5 MHz
System clock 2, 10 MHz

Fig. 7


Furnish integrated circuit to test
700
Furnish independent interface converter
710
Connect converter to integrated circuit
720
Connect converter to controller
730
Connect converter to command/ control center
740
Select mode
750
Transmit/receive data to/from test circuit
760
Transmit/receive data to/from Ethernet controller
770
Synchronize data
775
Adjust clock signals
780
Start/stop clock signals as necessary
785
Interface data to/ from integrated circuit and Ethernet controller
790

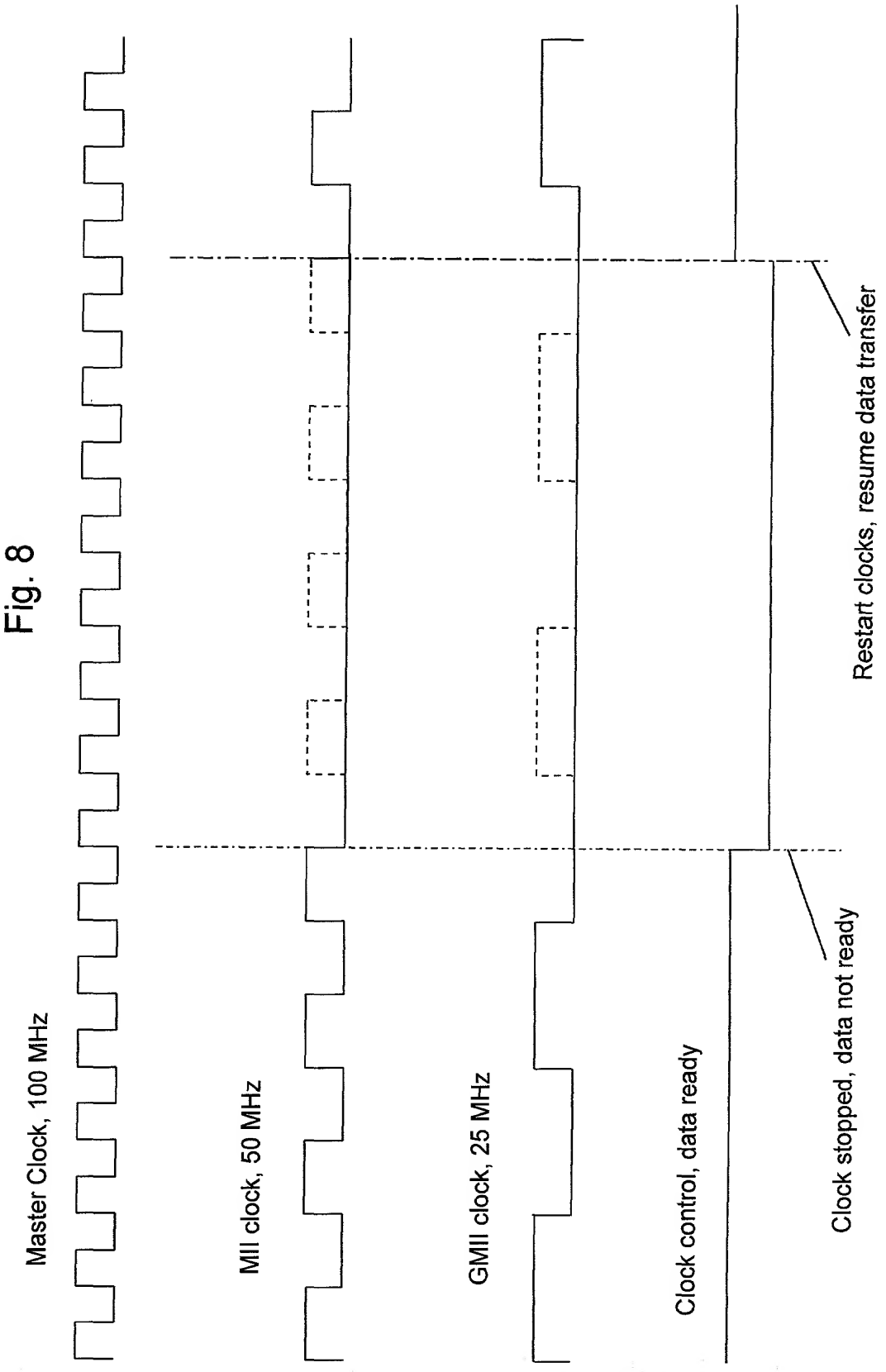

Master Clock, 100 MHz
MII clock, 50 MHz
GMII clock, 25 MHz
Clock control, data ready
Clock stopped, data not ready
Restart clocks, resume data transfer

Fig. 8

Fig. 9

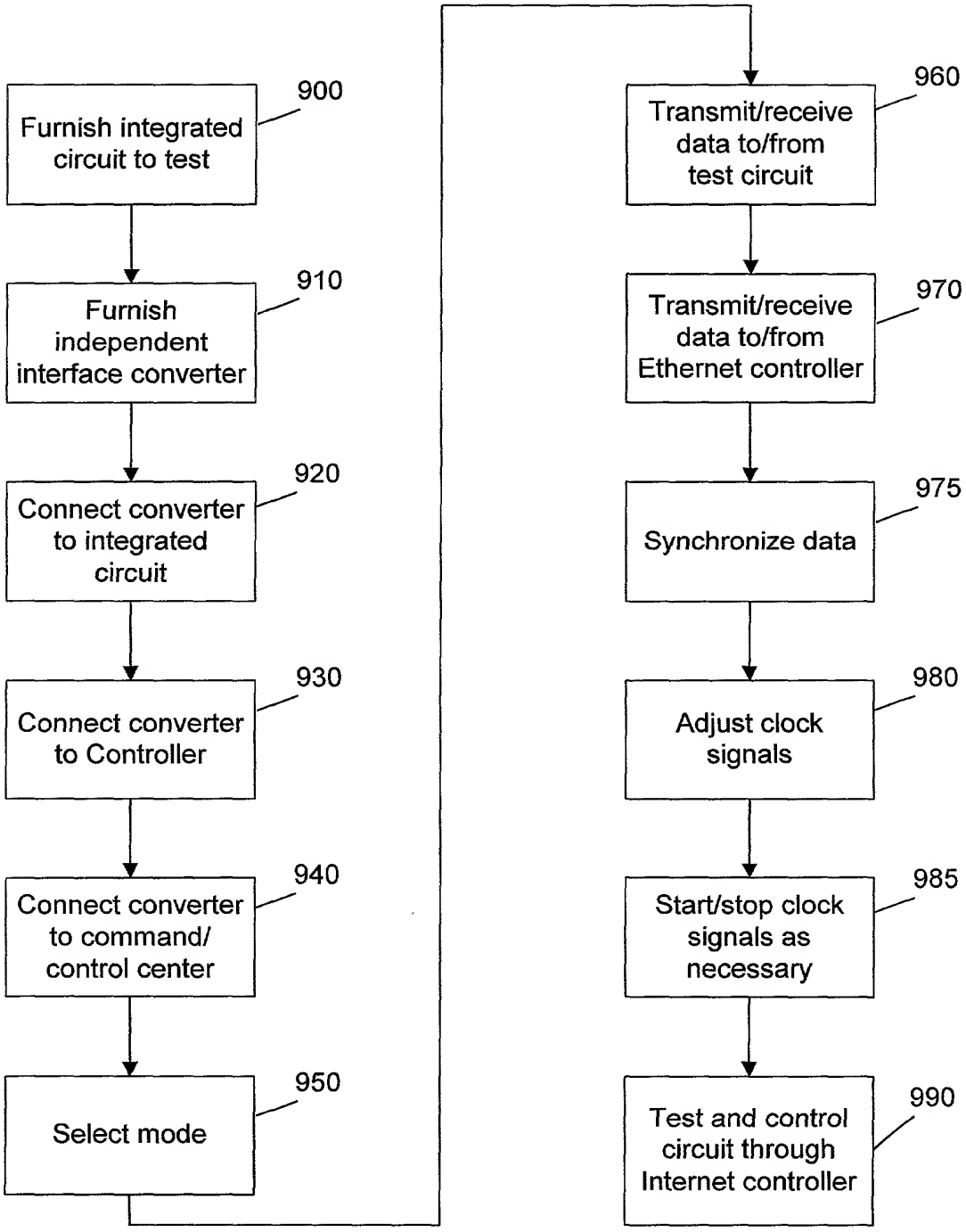
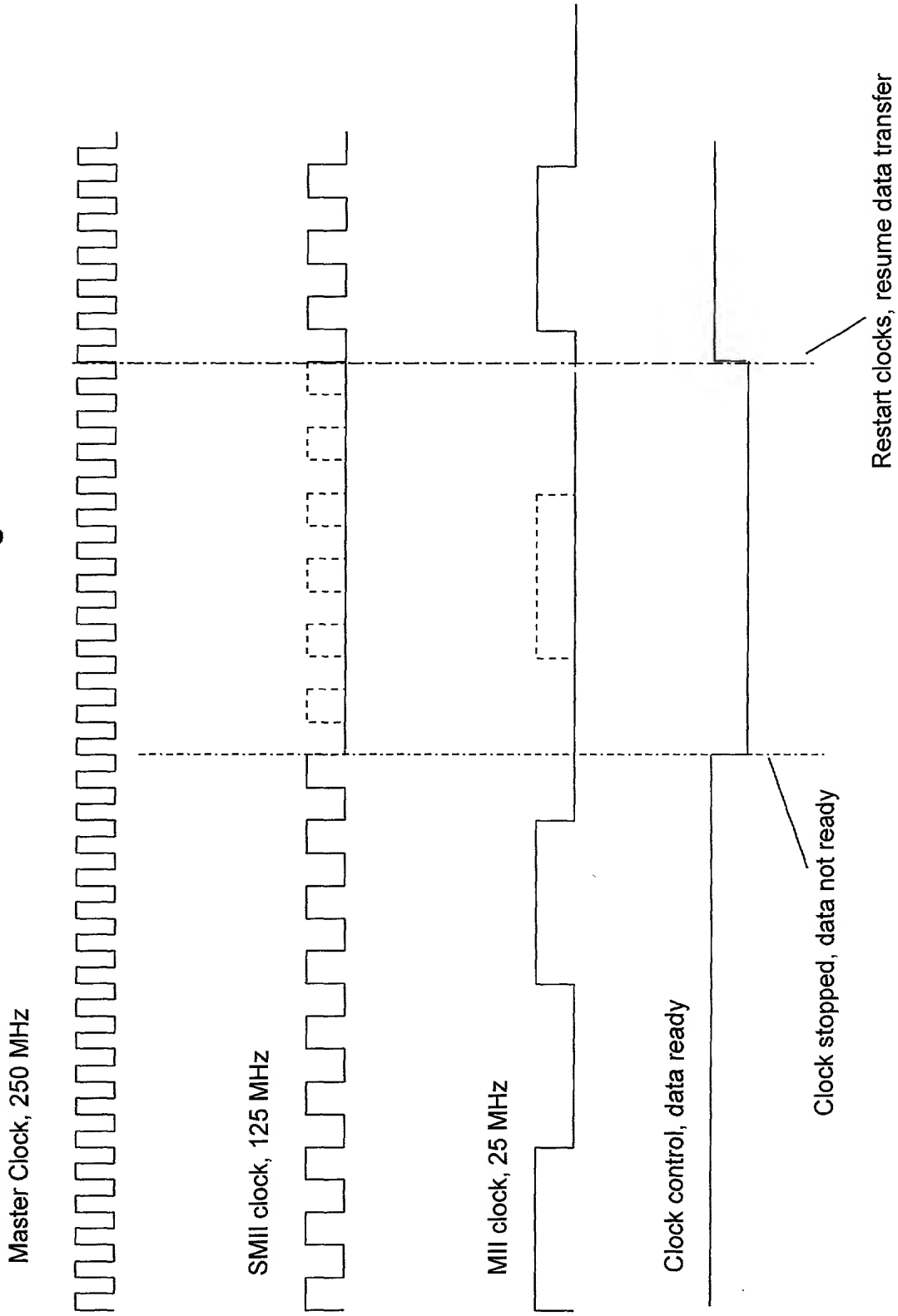

Furnish integrated circuit to test
900
Furnish independent interface converter
910
Connect converter to integrated circuit
920
Connect converter to Controller
930
Connect converter to command/ control center
940
Select mode
950
Transmit/receive data to/from test circuit
960
Transmit/receive data to/from Ethernet controller
970
Synchronize data
975
Adjust clock signals
980
Start/stop clock signals as necessary
985
Test and control circuit through Internet controller
990

Fig. 10


Master Clock, 250 MHz
SMII clock, 125 MHz
MII clock, 25 MHz
Clock control, data ready
Clock stopped, data not ready
Restart clocks, resume data transfer